Refine Search

Search Results -

Terms	Documents
L2 and (bus same (system or network))	14

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Friday, August 06, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L4	L2 and (bus same (system or network))	14	L4
L3	L2 and ((system adj1 bus) same (network adj1 bus))	0	L3
L2	L1 same microengine	14	L2
L1	multithread$3 near5 (processor or computer)	329	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2 and (bus same (system or network))	14

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Friday, August 06, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L4	L2 and (bus same (system or network))	14	L4
L3	L2 and ((system adj1 bus) same (network adj1 bus))	0	L3
L2	L1 same microengine	14	L2
L1	multithread$3 near5 (processor or computer)	329	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L4	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Friday, August 06, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L4	0	L5
DB=USPT,USOC; PLUR=YES; OP=OR			
L4	L2 and (bus same (system or network))	14	L4
L3	L2 and ((system adj1 bus) same (network adj1 bus))	0	L3
L2	L1 same microengine	14	L2
L1	multithread$3 near5 (processor or computer)	329	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(multithread$3 adj1 processor) same microengine	14

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, August 06, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L1	(multithread$3 adj1 processor) same microengine	14	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(multithread$3 adj1 processor) same microengine	2

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, August 06, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(multithread$3 adj1 processor) same microengine	2	L2
DB=USPT,USOC; PLUR=YES; OP=OR			
L1	(multithread$3 adj1 processor) same microengine	14	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
6668371.pn. or 6661794.pn. or 6625654.pn. or 6606704.pn.	4

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, August 06, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L1	6668371.pn. or 6661794.pn. or 6625654.pn. or 6606704.pn.	4	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(370/910 |370/912 |709/230 |709/200 |709/245 |709/220 |710/39 |710/52 |710/100 |710/260 |710/310 |710/5 |710/300 |710/34 |711/154 |711/100 |711/101 |712/244 |712/225 |712/10 |712/220).ccls.	9482

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L1	710/39,52,100,260,310,5,300,34;709/230,200,245,220;711/154,100,101;712/244,225,10,220;370

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L3	10

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L4	l1 and L3
L3	L2 and microengine
L2	multithread$3 near5 (processor or computer)
L1	710/39,52,100,260,310,5,300,34;709/230,200,245,220;711/154,100,101;712/244,225,10,220;370,

END OF SEARCH HISTORY

h e b b cg b e e ch

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6668371 B2

L1: Entry 1 of 4 File: USPT Dec 23, 2003

US-PAT-NO: 6668371
DOCUMENT-IDENTIFIER: US 6668371 B2

TITLE: Method and apparatus for software component analysis

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 2. Document ID: US 6661794 B1

L1: Entry 2 of 4 File: USPT Dec 9, 2003

US-PAT-NO: 6661794
DOCUMENT-IDENTIFIER: US 6661794 B1

TITLE: Method and apparatus for gigabit packet assignment for multithreaded packet processing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 3. Document ID: US 6625654 B1

L1: Entry 3 of 4 File: USPT Sep 23, 2003

US-PAT-NO: 6625654
DOCUMENT-IDENTIFIER: US 6625654 B1

TITLE: Thread signaling in multi-threaded network processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 4. Document ID: US 6606704 B1

L1: Entry 4 of 4 File: USPT Aug 12, 2003

US-PAT-NO: 6606704
DOCUMENT-IDENTIFIER: US 6606704 B1

h e b b g e e e f e e bb ef b e

TITLE: Parallel multithreaded processor with plural microengines executing multiple threads each microengine having loadable microcode

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw. De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
6668371.pn. or 6661794.pn. or 6625654.pn. or 6606704.pn.	4

Display Format: TI Change Format

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h e b b g e e e f e e bb ef b e

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L1: Entry 2 of 4 File: USPT Dec 9, 2003

US-PAT-NO: 6661794
DOCUMENT-IDENTIFIER: US 6661794 B1

TITLE: Method and apparatus for gigabit packet assignment for multithreaded packet processing

DATE-ISSUED: December 9, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wolrich; Gilbert	Framingham	MA		
Bernstein; Debra	Sudbury	MA		
Adiletta; Matthew J.	Worc	MA		
Hooper; Donald F.	Shrewsbury	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 474650 [PALM]
DATE FILED: December 29, 1999

INT-CL: [07] H04 L 12/56

US-CL-ISSUED: 370/394; 370/412
US-CL-CURRENT: 370/394; 370/412

FIELD-OF-SEARCH: 370/389, 370/394, 370/412, 370/413, 370/428, 370/429, 710/52, 710/64

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5173897	December 1992	Schrodi et al.	
☐	5784649	July 1998	Begur et al.	395/872
☐	5797043	August 1998	Lewis et al.	395/876
☐	5978838	November 1999	Mohamed et al.	
☐	6157955	December 2000	Narad et al.	709/228

h e b b cg b cc e

☐	6434145	August 2002	Opsasnick et al.	370/394
☐	6532509	March 2003	Wolrich et al.	710/240

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 633 678	January 1995	EP	

ART-UNIT: 2665

PRIMARY-EXAMINER: Hsu; Alpus H.

ASSISTANT-EXAMINER: Nguyen; Toan

ATTY-AGENT-FIRM: Fish & Richardson P.C.

ABSTRACT:

A network processor that has multiple processing elements, each processing element supporting multiple simultaneous program threads with access to shared resources in an interface. Packet data is received from high-speed ports in segments and each segment is assigned to one of the program threads. Each packet may be assigned to a single program thread, two program threads, or a different program thread for segment of data in a packet. For the two program threads, one program thread can be used for header segment processing and the other program thread can be used for handling payload segment(s). Dedicated inputs for ready status and sequence numbers can provide assistance for receiving the packet data over a high speed port. The dedicated inputs are used to monitor ready flags from the high speed ports on a cycle-by-cycle basis. The sequence numbers are used by the assigned threads to maintain ordering of segments within a packet, as well as to order the writes of the complete packets to transmit queues.

27 Claims, 29 Drawing figures

Previous Doc Next Doc Go to Doc#

L1: Entry 3 of 4 File: USPT Sep 23, 2003

US-PAT-NO: 6625654
DOCUMENT-IDENTIFIER: US 6625654 B1

TITLE: Thread signaling in multi-threaded network processor

DATE-ISSUED: September 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wolrich; Gilbert	Framingham	MA		
Bernstein; Debra	Sudbury	MA		
Hooper; Donald	Shrewsbury	MA		
Adiletta; Matthew J.	Worc	MA		
Wheeler; William	Southboro	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 473799 [PALM]
DATE FILED: December 28, 1999

INT-CL: [07] G06 F 15/16

US-CL-ISSUED: 709/230; 709/200, 709/102, 709/245
US-CL-CURRENT: 709/230; 709/200, 709/245, 718/102

FIELD-OF-SEARCH: 709/200, 709/102, 709/245, 709/230, 713/155

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5627829	May 1997	Gleeson et al.	370/230
☐	5689566	November 1997	Nguyen	713/155
☐	5742782	April 1998	Ito et al.	712/210
☐	5983274	November 1999	Hyder et al.	709/230
☐	6085215	July 2000	Ramakrishnan et al.	709/102

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☐ 6212542 April 2001 Kahle et al. 709/102

OTHER PUBLICATIONS

Schmidt et al, "The Preformance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, Online! Nov. 13, 1998.
Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers"Proceedings of the 2000 International Conference on Parallel Processing, Toronto, Ontario, Canada. Aug. 21-24, 2000, pp. 362-369.
Turner, Jonathan et al., "Design of a High Performance Active Router," Internet Document, Online Mar. 18, 1999.
Gomez, J.C. et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the Trap Protocol,"Journal of Parallel and Dsitributed Computing, Academic Press, Duluth, MN, US, vol. 40, No. 1, Jan. 10, 1997 pp. 103-117.

ART-UNIT: 2143

PRIMARY-EXAMINER: Wiley; David

ASSISTANT-EXAMINER: Nguyen; Phuoc H.

ATTY-AGENT-FIRM: Fish & Richardson P.C.

ABSTRACT:

A parallel hardware-based multithreaded processor is described. The processor includes a general purpose processor that coordinates system functions and a plurality of microengines that support multiple program threads. The processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed than even bank or an odd bank of memory and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references. A program thread communication scheme for packet processing is also described.

16 Claims, 18 Drawing figures

Previous Doc Next Doc Go to Doc#

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End of Result Set

Generate Collection Print

L1: Entry 4 of 4 File: USPT Aug 12, 2003

US-PAT-NO: 6606704
DOCUMENT-IDENTIFIER: US 6606704 B1

TITLE: Parallel multithreaded processor with plural microengines executing multiple threads each microengine having loadable microcode

DATE-ISSUED: August 12, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Adiletta; Matthew J.	Worcester	MA		
Wolrich; Gilbert	Framingham	MA		
Wheeler; William	Southborough	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 387111 [PALM]
DATE FILED: August 31, 1999

INT-CL: [07] G06 F 9/24

US-CL-ISSUED: 712/248; 712/10, 712/228
US-CL-CURRENT: 712/248; 712/10, 712/228

FIELD-OF-SEARCH: 712/10-22, 712/225, 712/228, 712/248

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3478322	November 1969	Evans	712/248
☐	3792441	February 1974	Wymore et al.	712/248
☐	4514807	April 1985	Nogi	712/21
☐	4745544	May 1988	Renner et al.	712/11
☐	5915123	June 1999	Mirsky et al.	712/16
	6023742	February 2000	Ebeling et al.	712/17

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☐				
☐	6079008	June 2000	Clery, III	712/11
☐	6272616	August 2001	Fernando et al.	712/228

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
WO 94/15287	July 1994	WO	
WO 97/38372	October 1997	WO	

OTHER PUBLICATIONS

Wazlowski, M., Agarwal, L., Lee T., Smith, A., Lam, E., Athanas, P., Silverman, H., Ghosh, S., PRISM-II compiler and architecture, IEEE PRoceedings, Workshop on FPGAs for Custom Computing Machines, 1993, IEEE.*
Trimberger, S., Carberry, D., Johnson, A., Wong, J., A time-multiplexed FPGA, Proceedings of The 5.sup.th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997, IEEE.*
Haug, G., Rosenstiel, W., Reconfigurable hardware as shared resource for parallel threads, IEEE Symposium on FPGAs for Custom Computing Machines, 1998, IEEE.*
Hauser, J.R., Wawrzynek, J., Garp: a MIPS processor with a reconfigurable coprocessor, Proceedings of The 5.sup.th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997, IEEE.*
"Multithreaded Processor Architectures", IEEE Spectrum, 32 (1995) Aug., No. 8, New York, US, pp. 38-46.
"A Three Dimensional Register File For Superscalar Processors", M. Tremblay et al., IEEE Proceedings of the 28.sup.th Annual Hawaii Int'l Conference on Systems Sciences, 1995, pp. 191-201.
"A Processor Architecture For Horizon", M.R. Thistle et al., IEEE 1998, pp. 35-41.
"The M-Machine Multicomputer", M. Fillo et al., IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
"StrongARMing Portable Communications", T. Litch et al., IEEE Micro 1998, pp. 48-55.

ART-UNIT: 2183

PRIMARY-EXAMINER: Ellis; Richard L.

ATTY-AGENT-FIRM: Fish & Richardson P.C.

ABSTRACT:

A parallel hardware-based multithreaded processor is described. The processor includes a general purpose processor that coordinates system functions and a plurality of microengines that support multiple hardware threads. The processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references.

17 Claims, 23 Drawing figures

h e b b cg b cc e

L3: Entry 1 of 4 File: USPT Dec 23, 2003

US-PAT-NO: 6668317
DOCUMENT-IDENTIFIER: US 6668317 B1

TITLE: Microengine for parallel processor architecture

DATE-ISSUED: December 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bernstein; Debra	Sudbury	MA		
Hooper; Donald F.	Shrewsbury	MA		
Adiletta; Matthew J.	Worcester	MA		
Wolrich; Gilbert	Framingham	MA		
Wheeler; William	Southborough	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 387046 [PALM]
DATE FILED: August 31, 1999

INT-CL: [07] G06 F 9/48

US-CL-ISSUED: 712/245; 712/228
US-CL-CURRENT: 712/245; 712/228

FIELD-OF-SEARCH: 712/245, 712/228, 712/39, 712/40, 712/248, 709/213, 709/312

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3373408	March 1968	Ling	712/228
☐	3940745	February 1976	Sajeva	710/244
☐	5390329	February 1995	Gaertner et al.	709/108
☐	5542088	July 1996	Jennings et al.	709/103
☐	5557766	September 1996	Takiguchi et al.	710/260

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☐	5574922	November 1996	James	712/220
☐	5630130	May 1997	Perotto et al.	709/107
☐	5680641	October 1997	Sidman	395/840
☐	5742822	April 1998	Motomura	709/102
☐	5761522	June 1998	Hisanaga et al.	709/107
☐	5812868	September 1998	Moyer et al.	712/23
☐	5854922	December 1998	Gravenstein et al.	712/245
☐	5937187	August 1999	Kosche et al.	709/104
☐	6195676	February 2001	Spix et al.	709/107
☐	6216220	April 2001	Hwang	709/103
☐	6223279	April 2001	Nishimura et al.	712/228
☐	6389449	May 2002	Nemirovsky et al.	709/108

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 745 933	April 1996	EP	
59111533	June 1984	JP	

OTHER PUBLICATIONS

"Multithreaded Processor Architectures", G.T. Byrd et al., IEEE Spectrum, IEEE Inc., New York, US, vol. 32, No. 8, Aug. 1, 1995, pps. 38-46.
"A Processor Architecture For Horizon", M.R. Thistle et al., Orlando, Washington, IEEE Comp. Soc. Press., US, vol. Conf. 1, Nov. 14, 1988, pps. 35-41.
"Strongarming Portable Communications", T. Litch et al., IEEE Micro, US, IEEE, Inc., New York, vol. 18, No. 2, Mar. 1, 1998, pps. 48-55.

ART-UNIT: 2183

PRIMARY-EXAMINER: Coleman; Eric

ATTY-AGENT-FIRM: Fish & Richardson P.C.

ABSTRACT:

A parallel hardware-based multithreaded processor is described. The processor includes a general purpose processor that coordinates system functions and a plurality of microengines that support multiple hardware threads. The processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references.

41 Claims, 23 Drawing figures

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 6587906 B2, US 20030105901 A1

Using default format because multiple data bases are involved.

L2: Entry 1 of 2 File: DWPI Jul 1, 2003

DERWENT-ACC-NO: 2003-645161
DERWENT-WEEK: 200361
COPYRIGHT 2004 DERWENT INFORMATION LTD
TITLE: Parallel multithreaded processor system for real-time operating system, has global command arbiter connected to microengine and system resource unit, to determine whether particular microengine command request is to be granted

INVENTOR: ADILETTA, M J; BERNSTEIN, D ; WHEELER, W ; WOLRICH, G

PRIORITY-DATA: 1999US-0470541 (December 22, 1999), 2003US-0339221 (January 9, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6587906 B2	July 1, 2003		000	G06F013/00
US 20030105901 A1	June 5, 2003		012	G06F013/14

INT-CL (IPC): G06 F 13/00; G06 F 13/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 2. Document ID: US 6671827 B2, US 20020083373 A1

L2: Entry 2 of 2 File: DWPI Dec 30, 2003

DERWENT-ACC-NO: 2002-681466
DERWENT-WEEK: 200402
COPYRIGHT 2004 DERWENT INFORMATION LTD

TITLE: Code debugging method for hardware-based multithreaded processor, involves writing current thread execution states to journal routine, if program execution in selected microengine encounters journal write command

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

h e b b g e e e f e g ef b e

Terms	Documents
(multithread$3 adj1 processor) same microengine	2

Display Format: - Change Format

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: US 6415338 B1

Using default format because multiple data bases are involved.

L1: Entry 1 of 5 File: USPT Jul 2, 2002

US-PAT-NO: 6415338
DOCUMENT-IDENTIFIER: US 6415338 B1

TITLE: System for writing a data value at a starting address to a number of consecutive locations equal to a segment length identifier

DATE-ISSUED: July 2, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Habot; Ronen	Ocean	NJ		

US-CL-CURRENT: 710/22; 710/25, 710/26, 710/5, 711/171

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWMC | Draw De

☐ 2. Document ID: US 6345334 B1

L1: Entry 2 of 5 File: USPT Feb 5, 2002

US-PAT-NO: 6345334
DOCUMENT-IDENTIFIER: US 6345334 B1

TITLE: High speed semiconductor memory device capable of changing data sequence for burst transmission

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWMC | Draw De

☐ 3. Document ID: US 5459842 A

L1: Entry 3 of 5 File: USPT Oct 17, 1995

US-PAT-NO: 5459842
DOCUMENT-IDENTIFIER: US 5459842 A

TITLE: System for combining data from multiple CPU write requests via buffers and using read-modify-write operation to write the combined data to the memory

h e b b g e e e f e ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 4. Document ID: US 5392412 A

L1: Entry 4 of 5 File: USPT Feb 21, 1995

US-PAT-NO: 5392412
DOCUMENT-IDENTIFIER: US 5392412 A

TITLE: Data communication controller for use with a single-port data packet buffer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 5. Document ID: US 5392391 A

L1: Entry 5 of 5 File: USPT Feb 21, 1995

US-PAT-NO: 5392391
DOCUMENT-IDENTIFIER: US 5392391 A

TITLE: High performance graphics applications controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
5392412.pn. or 5392391.pn. or 5459842.pn. or 6415338.pn. or 6345334.pn.	5

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☐ 1. Document ID: US 6728845 B2

Using default format because multiple data bases are involved.

L4: Entry 1 of 10 File: USPT Apr 27, 2004

US-PAT-NO: 6728845
DOCUMENT-IDENTIFIER: US 6728845 B2

TITLE: SRAM controller for parallel processor architecture and method for controlling access to a RAM using read and read/write queues

DATE-ISSUED: April 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Adiletta; Matthew J.	Worcester	MA		
Wheeler; William	Southborough	MA		
Redfield; James	Hudson	MA		
Cutter; Daniel	Townsend	MA		
Wolrich; Gilbert	Framingham	MA		

US-CL-CURRENT: 711/154; 710/39, 711/158

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 2. Document ID: US 6681300 B2

L4: Entry 2 of 10 File: USPT Jan 20, 2004

US-PAT-NO: 6681300
DOCUMENT-IDENTIFIER: US 6681300 B2

TITLE: Read lock miss control and queue management

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 3. Document ID: US 6631462 B1

L4: Entry 3 of 10 File: USPT Oct 7, 2003

US-PAT-NO: 6631462

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DOCUMENT-IDENTIFIER: US 6631462 B1

TITLE: Memory shared between processing threads

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 4. Document ID: US 6631430 B1

L4: Entry 4 of 10 File: USPT Oct 7, 2003

US-PAT-NO: 6631430
DOCUMENT-IDENTIFIER: US 6631430 B1

TITLE: Optimizations to receive packet status from fifo bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 5. Document ID: US 6625654 B1

L4: Entry 5 of 10 File: USPT Sep 23, 2003

US-PAT-NO: 6625654
DOCUMENT-IDENTIFIER: US 6625654 B1

TITLE: Thread signaling in multi-threaded network processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 6. Document ID: US 6606704 B1

L4: Entry 6 of 10 File: USPT Aug 12, 2003

US-PAT-NO: 6606704
DOCUMENT-IDENTIFIER: US 6606704 B1

TITLE: Parallel multithreaded processor with plural microengines executing multiple threads each microengine having loadable microcode

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 7. Document ID: US 6587906 B2

L4: Entry 7 of 10 File: USPT Jul 1, 2003

US-PAT-NO: 6587906
DOCUMENT-IDENTIFIER: US 6587906 B2

TITLE: Parallel multi-threaded processing

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 8. Document ID: US 6560667 B1

L4: Entry 8 of 10 File: USPT May 6, 2003

US-PAT-NO: 6560667
DOCUMENT-IDENTIFIER: US 6560667 B1

TITLE: Handling contiguous memory references in a multi-queue system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 9. Document ID: US 6532509 B1

L4: Entry 9 of 10 File: USPT Mar 11, 2003

US-PAT-NO: 6532509
DOCUMENT-IDENTIFIER: US 6532509 B1

TITLE: Arbitrating command requests in a parallel multi-threaded processing system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 10. Document ID: US 6427196 B1

L4: Entry 10 of 10 File: USPT Jul 30, 2002

US-PAT-NO: 6427196
DOCUMENT-IDENTIFIER: US 6427196 B1
** See image for Certificate of Correction **

TITLE: SRAM controller for parallel processor architecture including address and command queue and arbiter

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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Terms	Documents
L1 and L3	10

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US006587906B2

(12) **United States Patent**
Wolrich et al.

(10) **Patent No.: US 6,587,906 B2**
(45) **Date of Patent: Jul. 1, 2003**

(54) **PARALLEL MULTI-THREADED PROCESSING**

(75) Inventors: **Gilbert Wolrich**, Framingham, MA (US); **Debra Bernstein**, Sudbury, MA (US); **Matthew J. Adiletta**, Worcester, MA (US); **William Wheeler**, Southborough, MA (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/339,221**

(22) Filed: **Jan. 9, 2003**

(65) **Prior Publication Data**

US 2003/0105901 A1 Jun. 5, 2003

Related U.S. Application Data

(63) Continuation of application No. 09/470,541, filed on Dec. 22, 1999, now Pat. No. 6,532,509.

(51) **Int. Cl.**[7] **G06F 13/00**; G06F 13/14

(52) **U.S. Cl.** **710/240**; 710/52; 709/104

(58) **Field of Search** 710/240–244, 710/200, 40, 107, 52, 56, 20, 7, 105, 313, 310, 712/32, 36; 370/464, 910; 709/231, 200, 201, 217, 104; 711/150, 151, 148

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6,347,344	B1 *	2/2002	Baker et al.
6,532,509	*	3/2003	Wolrich et al.

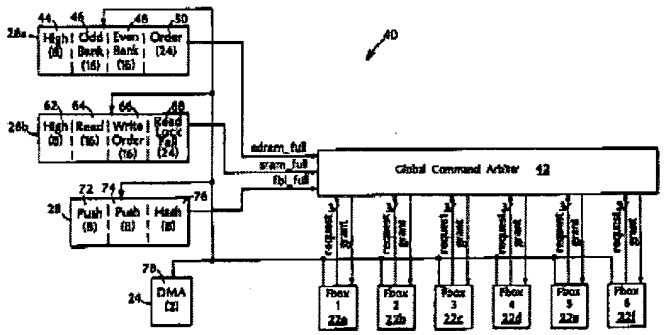
* cited by examiner

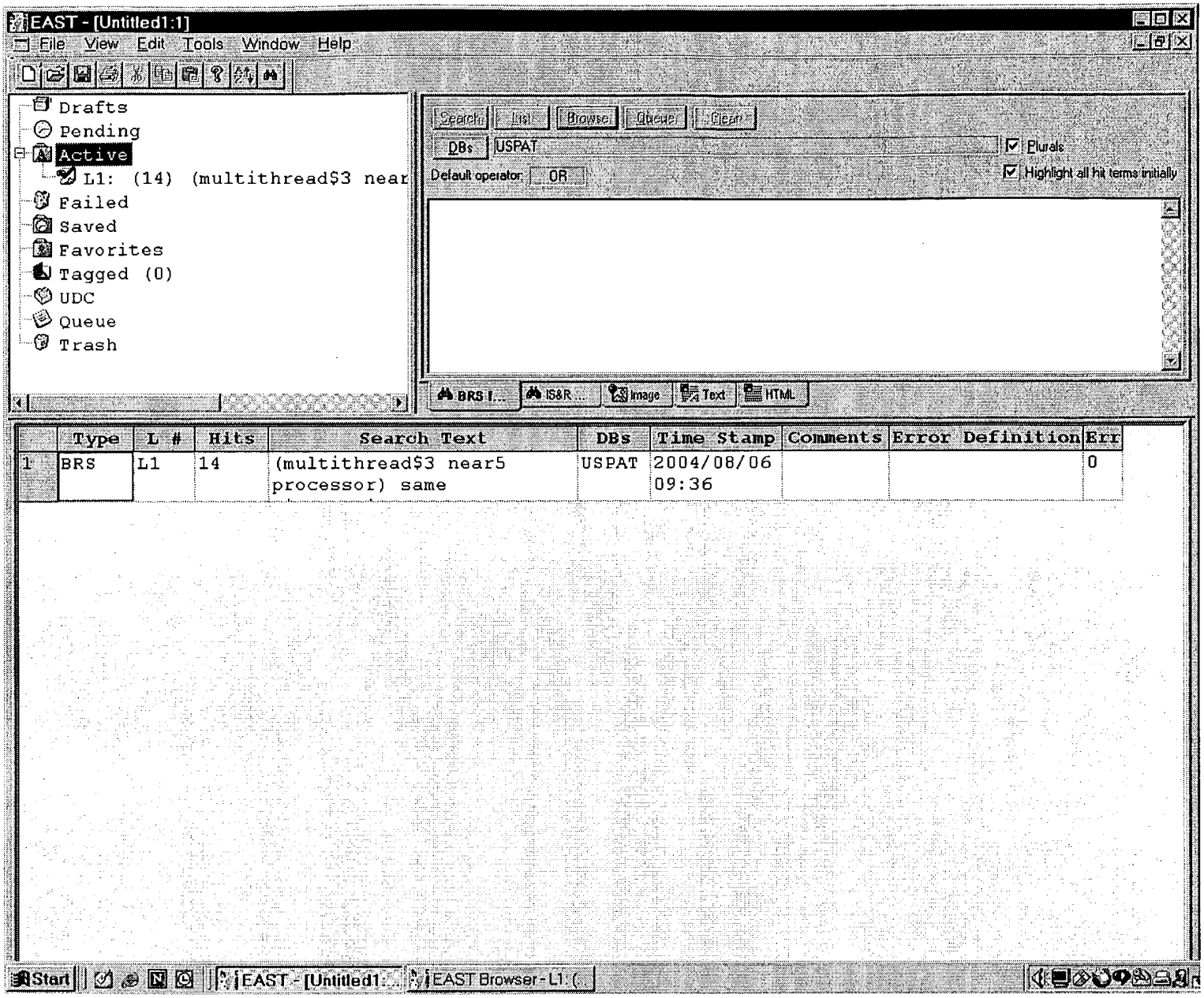
Primary Examiner—Gopal C. Ray
(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(57) **ABSTRACT**

A parallel, multi-threaded processor system and technique for arbitrating command requests is described. The system includes a plurality of microengines, a plurality of shared system resources and a global command arbiter. The global command arbiter uses a command request protocol that is based on the shared system resources and command type to grant or deny a microengine command request for a shared resource.

17 Claims, 4 Drawing Sheets

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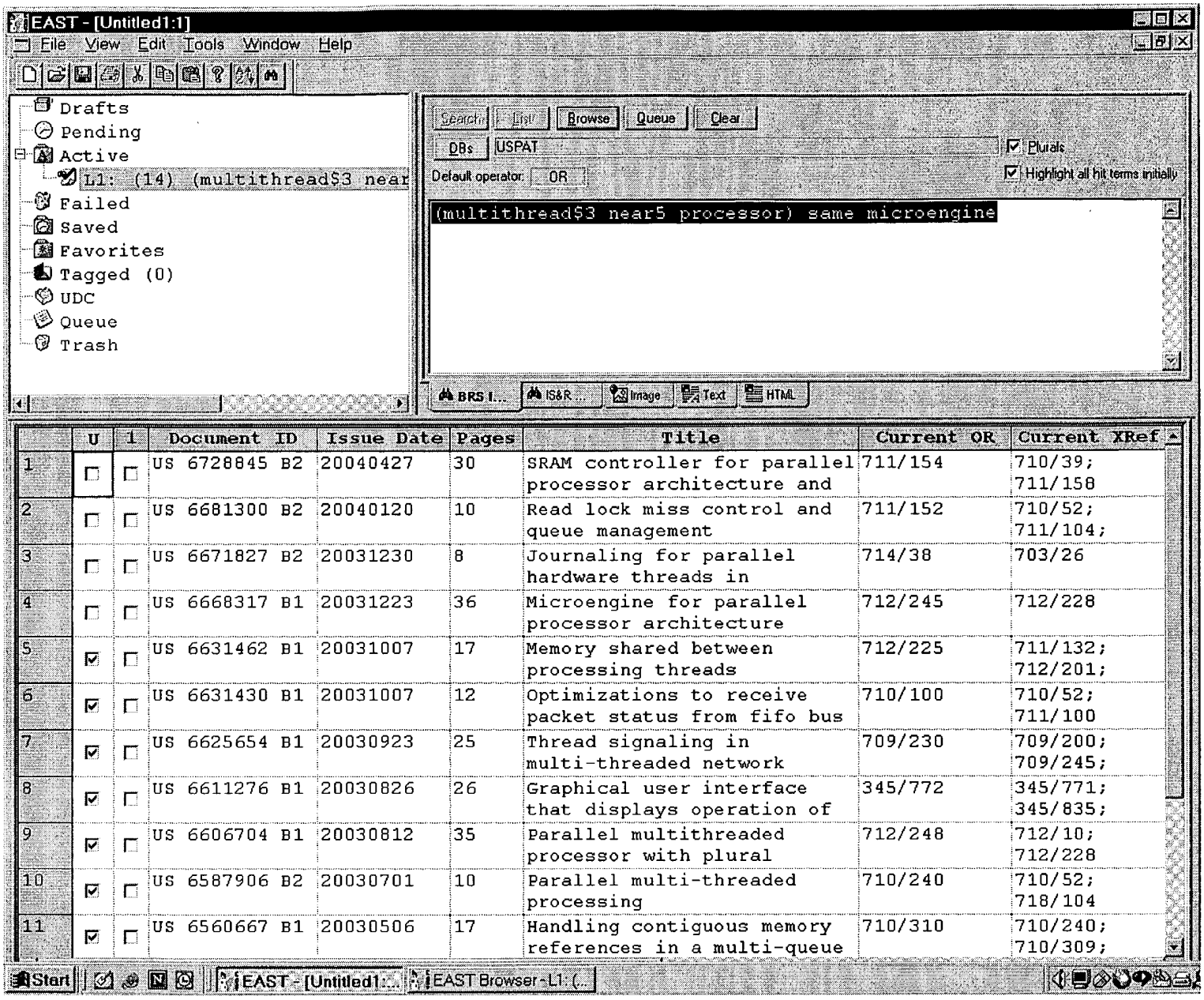

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6728845 B2	20040427	30	SRAM controller for parallel processor architecture and	711/154	710/39; 711/158
2	☐	☐	US 6681300 B2	20040120	10	Read lock miss control and queue management	711/152	710/52; 711/104;
3	☐	☐	US 6671827 B2	20031230	8	Journaling for parallel hardware threads in	714/38	703/26
4	☐	☐	US 6668317 B1	20031223	36	Microengine for parallel processor architecture	712/245	712/228
5	☑	☐	US 6631462 B1	20031007	17	Memory shared between processing threads	712/225	711/132; 712/201;
6	☑	☐	US 6631430 B1	20031007	12	Optimizations to receive packet status from fifo bus	710/100	710/52; 711/100
7	☑	☐	US 6625654 B1	20030923	25	Thread signaling in multi-threaded network	709/230	709/200; 709/245;
8	☑	☐	US 6611276 B1	20030826	26	Graphical user interface that displays operation of	345/772	345/771; 345/835;
9	☑	☐	US 6606704 B1	20030812	35	Parallel multithreaded processor with plural	712/248	712/10; 712/228
10	☑	☐	US 6587906 B2	20030701	10	Parallel multi-threaded processing	710/240	710/52; 718/104
11	☑	☐	US 6560667 B1	20030506	17	Handling contiguous memory references in a multi-queue	710/310	710/240; 710/309;

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1 **A single-chip programmable platform based on a multithreaded processor and configurable logic clusters**
Young-Don Bae; Seong-Il Park; In-Cheol Park;
Solid-State Circuits, IEEE Journal of , Volume: 38 , Issue: 10 , Oct. 2003
Pages:1703 - 1711

[Abstract] [PDF Full-Text (715 KB)] **IEEE JNL**

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2 **An efficient, protected message interface**
Whay Sing Lee; Dally, W.J.; Keckler, S.W.; Carter, N.P.; Chang, A.;
Computer , Volume: 31 , Issue: 11 , Nov. 1998
Pages:69 - 75

[Abstract] [PDF Full-Text (220 KB)] **IEEE JNL**

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3 **Nomadic Threads: a migrating multithreaded approach to remote memory accesses in multiprocessors**
Jenks, S.; Gaudiot, J.-L.;
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[Abstract] [PDF Full-Text (1084 KB)] **IEEE CNF**

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7 **Advanced medical instrument-oriented operating system**
Mouyong Liu; Yue Wu; Jiguang Ge;
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8 **Experience with executing shared memory programs using fine-gra communication and multithreading in EM-4**
Sato, M.; Kodama, Y.; Sakai, S.; Yamaguchi, Y.;
Parallel Processing Symposium, 1994. Proceedings., Eighth International , 26 April 1994
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[Abstract] [PDF Full-Text (560 KB)] **IEEE CNF**

9 **Overview of the START(*T) multithreaded computer**
Beckerle, M.J.;
Compcon Spring '93, Digest of Papers. , 22-26 Feb. 1993
Pages:148 - 156

[Abstract] [PDF Full-Text (628 KB)] **IEEE CNF**

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Nomadic Threads: a migrating multithreaded approach to remote memory accesses in multiprocessors

Jenks, S. Gaudiot, J.-L.
Dept. of Electr. Eng. Syst., Univ. of Southern California, Los Angeles, CA, USA;

This paper appears in: **Parallel Architectures and Compilation Techniques, 1996., Proceedings of the 1996 Conference on**

Meeting Date: 10/20/1996 - 10/23/1996
Publication Date: 20-23 Oct. 1996
Location: Boston, MA USA
On page(s): 2 - 11
Reference Cited: 23
Number of Pages: xiv+304
Inspec Accession Number: 5425587

Abstract:
This paper describes an abstract **multithreaded** architecture for distributed **memory** multicomputers that significantly reduces the number of message transfers when compared to conventional "remote **memory** access" approaches instead of statically executing on its assigned **processor** and fetching data from remote storage, a Nomadic Thread transfers itself to the **processor** which contains the data it needs. This enables Nomadic Threads to take advantage of spatial locality found in the usage of many data

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structures, because the migration of a thread to a node makes access to surrounding data local. By reducing the number of messages and laking advantage of locality the Nomadic Threads approach allows programs to use fewer data transfers than conventional approaches while providing a simple runtime **interface** to compilers. The Nomadic Threads runtime system is currently implemented for the Thinking Machines Corp. Connection Machine 5 (CM5), but is portable to other distributed **memory** systems, including networks of workstations

Index Terms:

abstract data types distributed **memory** systems parallel architectures Nomadic Threads abstract **multithreaded** architecture compilers distributed **memory** multicomputers migrating **multithreaded** approach multiprocessors remote **memory** accesses runtime **interface** spatial locality

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Overview of the START(*T) multithreaded computer

Beckerle, M.J.
Motorola Cambridge Res. Center, Cambridge, MA, USA;

This paper appears in: **Compcon Spring '93, Digest of Papers.**

Meeting Date: 02/22/1993 - 02/26/1993
Publication Date: 22-26 Feb. 1993
Location: San Francisco, CA USA
On page(s): 148 - 156
Reference Cited: 9
Inspec Accession Number: 4750257

Abstract:
The author provides an overview of the START(*T) computer system being implemented by MIT and Motorola. *T is a scalable computer architecture designed to support a broad variety of parallel programming styles, including those which use **multithreading** to tolerate the increases in **memory** latency which occur as the machine size is scaled up. The hardware uses a customized reduced instruction set computer (RISC) microprocessor with a network messaging **interface** and synchronization unit tightly coupled into the **processor** architecture. This hardware is coupled with a high-performance network having a fat-tree topology with high cross-section bandwidth. In addition, a HIPPI I/O system provides access to the world of supercomputer-class I/O devices. An innovative

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software architecture is layered on this hardware to produce a working system which is at its foundation a UNIX-like software environment. The software architecture specifies the structure of parallel programs and the way that they can be controlled and debugged

Index Terms:

HIPPI I/O system START(*T) **multithreaded** computer UNIX-like software environment customised RISC microprocessor fat-tree topology **memory** latency network messaging **interface** overview parallel architectures parallel programming parallel programming styles programming environments scalable computer architecture software architecture synchronisation synchronization unit HIPPI I/O system START(*T) **multithreaded** computer UNIX-like software environment customised RISC microprocessor fat-tree topology **memory** latency network messaging **interface** overview parallel architectures parallel programming parallel programming styles programming environments scalable computer architecture software architecture synchronisation synchronization unit

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